Company Overview

- **Engineering firm located in Edina, MN**
- **Focusing on FPGA DSP Logic Design**
- **Founded in 1989**
- **World wide IP Core provider**
- **Created world's fastest FFT IP Core**
- **PareCore Architect™ for IP Design**
- **Concept to Product Design Flow**
- **Complete radar processing in single FPGA**
- **OFDM Transceivers**
- **Software defined radios**
- **Image compression and processing**
- **Revenue growth of 60% each of last 3 years**

Clients

- **Raytheon Company**
- **BAE Systems**
- **ITT Industries**
- **NASA**
- **Intellon Corporation**
- **Phase IV Systems**
- **DRS Communications**
- **Transoma Medical**
- **General Dynamics**

- **Allied Signal (Honeywell)**
- **Motorola SPS**
- **InterScience Corporation**
- **MindPlay LLC**
- **Smiths Aerospace**
- **Sandia Corporation**
- **Herrick Technical Labs**
- **SED Systems**
- **Bally Gaming**

Business Model

- **FPGA Design Consulting Services**
- **Retain IP Rights to re-usable logic**
- **Build line of high performance configurable IP Cores**
- **Continue ParaCore Development**
- **Market, Sell, and Support IP Cores**
- **Design and deliver the highest performance DSP algorithms in FPGAs**
- **Design and deliver custom reconfigurable computing platforms**

IP Core Status

- **World's fastest FFT/IFFT**
- **Convolution Kernel**
- **Floating Point Library**
- **Floating Point FFT/IFFT**
- **Ultra Long FFT/IFFT including external memory interface**
- **Split Radix FFT/IFFT**
- **2D FFT/IFFT including external memory interface**
- **AES Encryption/Decryption**

ParaCore Design Goals

- **Ultra fast proof of concept (virtual prototype)**
- **Use virtual prototype to test IP**
- **Thorough and automatic test bench**
- **Tight link to simulation/synthesis**
- **Library of proven IP used as building blocks**
- **Versatile IP – Parametric and scalable**

Design Flow

- **Specification**
- **Virtual Prototype**
- **ParaCore Logic Design**
- **Functional simulation and test**
- **Build to target technology**
- **Timing simulation and test**
- **Delivery IP Core to client**
- **Create re-usable IP Core**

Full Design Flow

Client Test Data

ParaCore Virtual Prototype

ParaCore IP Environment
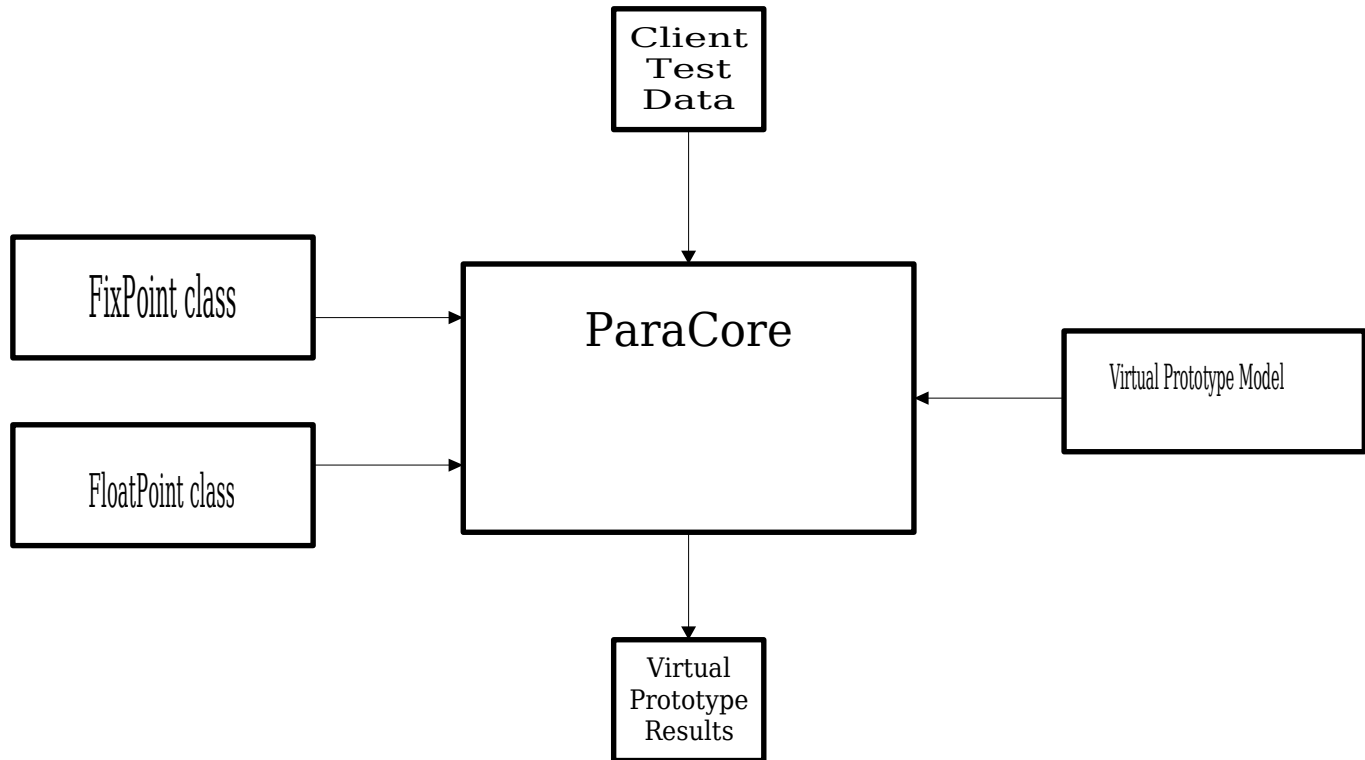
Client Approval

Compare
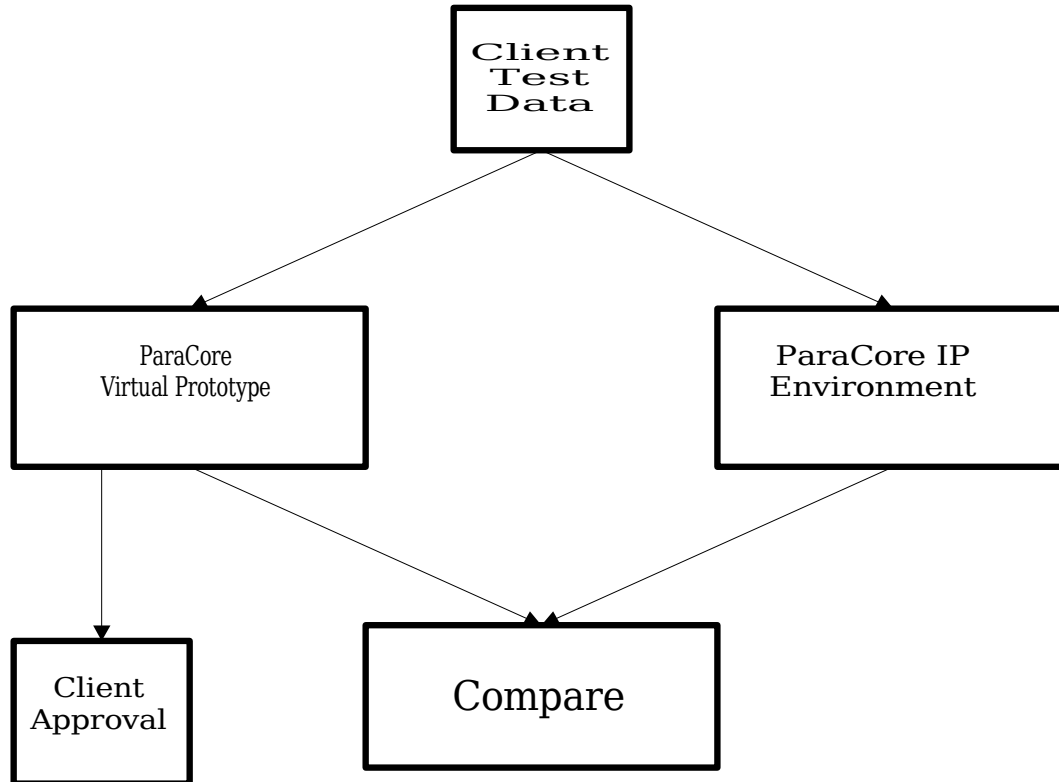
Virtual Prototype Benefits

- **Ultra fast concept to results**
- **Implement functionality of specification prior to logic design**
- **Solve design issues as early as possible in design cycle**
- **Bit for bit result tracking of FPGA implementation**
- **Results applied to FPGA logic test bench to guarantee accuracy**

Virtual Prototype

Math results exactly match ASIC/FPGA implementation

ParaCore Architect

- **Parametric IP Creation**
- **Complete Object Oriented Design**
- **Simple modification**
- **Full library of parametric functions**
- **Auto HDL generation**
- **Auto test bench creation**
- **Completely overcomes HDL limitations**

ParaCore Design Flow