Mixed-Radix FFT IP Core (FFT_MIXED)

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Features

- Fast Fourier Transform (FFT) for non-power of 2 lengths.
- Any combination of radix-2, -3, -5, and -7.
- Run-time selectable length within superset
- Example mixed length: 32x3x5 = 480-point
- Run-time selectable Forward/Inverse transform mode
- Any width fixed- or floating-point
- Single- or multi-stream I/O
- Continuous processing performance
- See Table 1 for 3-stream 768 point FFT.
- Customized for any order inputs and outputs
- Includes C/C++ bit-accurate model and data generator
- Model also usable from MATLAB
- Includes Verilog testbench and run scripts

Core Facts

Provided with Core	
Documentation	User Guide
Design File Formats	ISE Project with EDIF/NGC netlist, Verilog source available for extra cost
Constraints Files	.ucf constraints
Verification	Verilog Testbench, Test Vectors
Instantiation Templates	Verilog
Reference Designs & Application Notes	None
Additional Items	C/C++ Model
Simulation Tool Used	
Aldec Riviera 2008.06	
Support	
Support Provided by Dillon Engineering, Inc.	

Table 1: Example Implementation Statistics for Xilinx® FPGAs: Continuous 3-stream 768 point (256x3) FFT, 16-bit complex fixed-point

Family	Example Device	Fmax (MHz)	Slice FF[1]	Slice LUT[1]	IOB[2]	GCLK	BRAM	MULT/ DSP48/E	DCM & MGT	Design Tools
Spartan®-3A	XC3SD3400A-5	100	9,673	10,956	207	1	13	62	N/A	ISE® 10.1.02
Virtex®-4	XC4VSX55-12	180	10,435	11,842	207	1	13	62	N/A	ISE® 10.1.02
Virtex®-5	XC5VSX50T-3	240	10,935	12,722	207	1	8	62	N/A	ISE® 10.1.02

Notes:

1) Actual slice count dependent on percentage of unrelated logic – see Mapping Report File for details

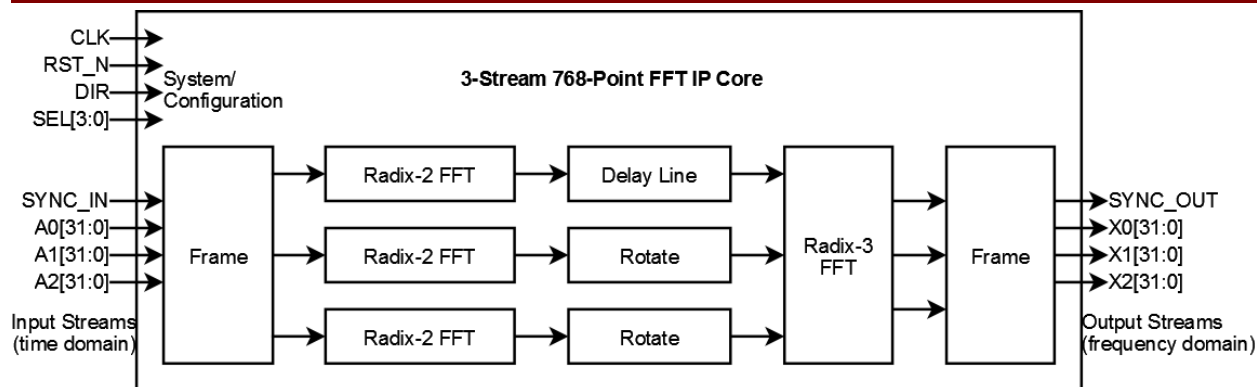2) Assuming all core I/Os and clocks are routed off-chip.

Figure 1: Mixed-Radix FFT Block Diagram

General Description

Dillon Engineering's Mixed-Radix FFT IP Core uses a modular combination of radix-2, -3, -5, and -7 Fast Fourier Transform (FFT) pipelined engines to provide discrete transforms on data frames or continuous data streams, with sample rate up to the maximum clock frequency. The engines are arranged to provide the most beneficial resource usage and data ordering for the system. The IP Core is further customized to support single- or multi-stream continuous throughput I/O, and any width fixed- or floating-point data.

Functional Description

Frame

The Frame blocks use control signaling to delimit discrete data frames per the selected transform length.

Radix-2 FFT

In the case of the 768-point example, each radix-2 FFT engine supports up to 256 length, using a Decimation-in-Frequency (DIF) form to take in natural-ordered inputs split among the 3 streams.

Rotate/Delay Line

In order to provide natural-order outputs on the proper streams, 2 of the streams contain an additional rotation stage by way of a custom CORDIC engine and twiddle multiply. A delay line on the top stream is used to align data into the radix-3 engine. The rotation stage can be eliminated in prime factor FFTs, resulting in different output ordering. Additional re-ordering and rotation stages may be required in other mixed-radix combinations.

Radix-3 FFT

In the case of the 768-point example, each radix-3 engine supports a 3-point FFT, using a Decimation-in-Time (DIT) form to provide natural-ordered outputs split among the 3 streams.

Applications

The Pipelined Floating Point FFT IP Core is useful in High Performance Embedded Computing (HPEC) applications which require continuous Digital Signal Processing (DSP) at high sample rates. Mixed-radix FFT is often required in many radio communication coding schemes. End applications and markets include radar, sonar, spectral analysis, and telecommunications.

Core Modifications

The IP Core is available in netlist or parameterized source code and supports the following:

- Netlist builds for any Xilinx device. FFT length and speed depend on chip resources and speed grade.

- Per-transform length selectable in powers-of-X for each radix-X supported.

- Per-transform mode selectable between Forward and Inverse FFT.

- Static length and mode configuration. Pipeline must be clear before changing these configuration settings.

- Any-width fixed-point or IEEE-754 single- or custom-precision floating point math operators using Xilinx Coregen floating point cores. Options for various scaling, rounding and saturation modes, all matched bit-accurate with the C/C++-model.

- Combinations of Decimation-in-Frequency (DIF), Decimation-in-time (DIT), mixed-radix and prime factor FFT providing optimal resource usage and ordering of data inputs and outputs for the system.

Core I/O Signals

The core signal I/O have not been fixed to specific device pins to provide flexibility for interfacing with user logic. Descriptions of all signal I/O are provided in Table 2.

Table 2: Core I/O Signals.

Signal	Signal Direction	Description
CLK	Input	Clock Input. Single source used for all I/O and internal clocking.
RST_N	Input	Active-low asynchronous reset. Resets all control logic.
DIR	Input	Transform mode select. 0 = Forward FFT, 1 = Inverse FFT.
SEL[3:0]	Input	Transform length select. Individual bits for each rank in the length superset.
SYNC_IN	Input	Input sync strobe. Indicates to the core to begin processing i_data on the following clock cycle.
A[31:0]	Input	Input data (per stream). Complex data of the form R + iQ, where R is contained in bits 31:16 and Q is contained in bits 15:0, each a signed integer for the fixed-point example.
SYNC_OUT	Output	Output sync strobe. Indicates the core is sending processed o_data beginning on the following clock cycle.
X[31:0]	Output	Output data (per stream). Complex data of the form R + iQ, where R is contained in bits 31:16 and Q is contained in bits 15:0, each a signed integer for the fixed-point example.

Critical Signal Descriptions

All interface and internal operation of the core is synchronous to CLK. Simple SYNC strobes are used on the input and output interfaces to signal that data is valid on the following clock cycle. An active SYNC coinciding with the last data point thus indicates back-to-back transforms. A SYNC_IN strobe active while the core is already inputing data is ignored. Tying SYNC_IN active will signal the core to perform continuous transforms, and SYNC_OUT will strobe as normal to frame the output data.
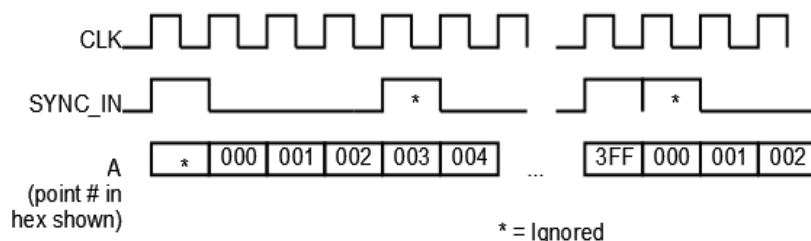
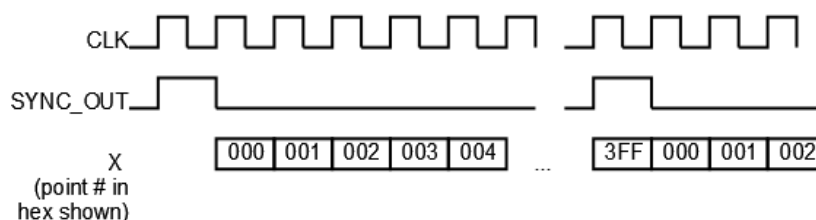**Figure 2: Interface Input Timing, 1K-Length Back-to-Back Transforms**

Figure 3: Interface Output Timing, 1K-Length Back-to-Back Transforms

The DIR and SEL configuration inputs are by default selectable per-transform, but must be stable starting with SYNC_IN active and must not be changed until the transformed data has been completely output from the core.

Core Assumptions

Following SYNC_IN, the initial transform has a start-up latency dependent on the re-ordering stages, the core math latencies and the length of the transform. The core provides continuous processing at steady state, though the SYNC IN to OUT latencies may vary slightly due to internal pipeline alignment.

Verification Methods

The core is verified to be bit-accurate with the C/C++ data model under all supported lengths, modes, throughputs and data format, using a rigorous simulation suite of directed and random data. Our model development is evaluated in terms of SQNR with a double-precision floating point software FFT implementation. Dillon Engineering's FFT IP Cores have been proven over the years in many Xilinx designs.

Ordering Information

This product is available directly from Dillon Engineering, Inc. Please contact Dillon Engineering for pricing and additional information about this product using the contact information on the front page of this datasheet.

Visit www.dilloneng.com/fft_ip to see all of Dillon Engineering's FFT IP offerings, including:

- UltraLong FFTs (up to 64M points, fixed or floating point)

- Parallel Butterfly FFTs (continuous FFTs at multiple points per clock cycle)

- Full Parallel FFTs (extremely fast rates, up to 25GSamples/sec)

- 2D FFTs (Two-dimensional transform for image processing)

Related Information

Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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