Dillon Engineering, Inc.

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Floating Point FFT/IFFT IP Core

Features

- Worlds fastest and most flexible Floating Point FFT IP Core
- Ultra high performance (> 1GSPS possible)
- Custom precision, any exponent and mantissa width
- Clock speeds over 200 MHz in Virtex II Pro
- IEEE 754 compliant
- Parametric IP core for maximum flexibility
- Available in generic HDL or targeted EDIF formats
- Full test bench supplied
- Any radix-2 or split radix lengths
- Mixed radix configurations - radix-2 x radix-3, radix-2 x radix-5, and radix-2 x radix-7
- Ultra long FFTs with external SRAM, both ZBT and DDR SRAM supported
- Naturally ordered I/O streams
- ParaCore Architect™ IP Core
- Massively parallel butterfly architecture
- FFT Development Kit supplied with IP

General Description

Dillon Engineering's (DE) Floating Point FFT IP Core (FpFft) is the most versatile available in the industry. It is designed to address the design challenges of digital signal processing in FPGA's today. It is the only floating point FFT IP Core can be tailored made to meet exact needs of your application.

By optimizing the mantissa and exponents lengths for the target technology and application, tremendous gains in dynamic range and precision can be attained versus the normal fixed point FFT results with a minimal impact on device size and cost.

The processing speed of the core is increased by adding butterfly structures in parallel. For ultra high performance applications, parallel data paths into and out of the module can be added to allow the system to maintain a reasonable clock rate. The speed of operation is only limited by the amount of available logic in the target device.

An FFT Development Kit provides C math modeling with bit accurate results and HDL simulation behavioral models which drastically improve simulation performance.

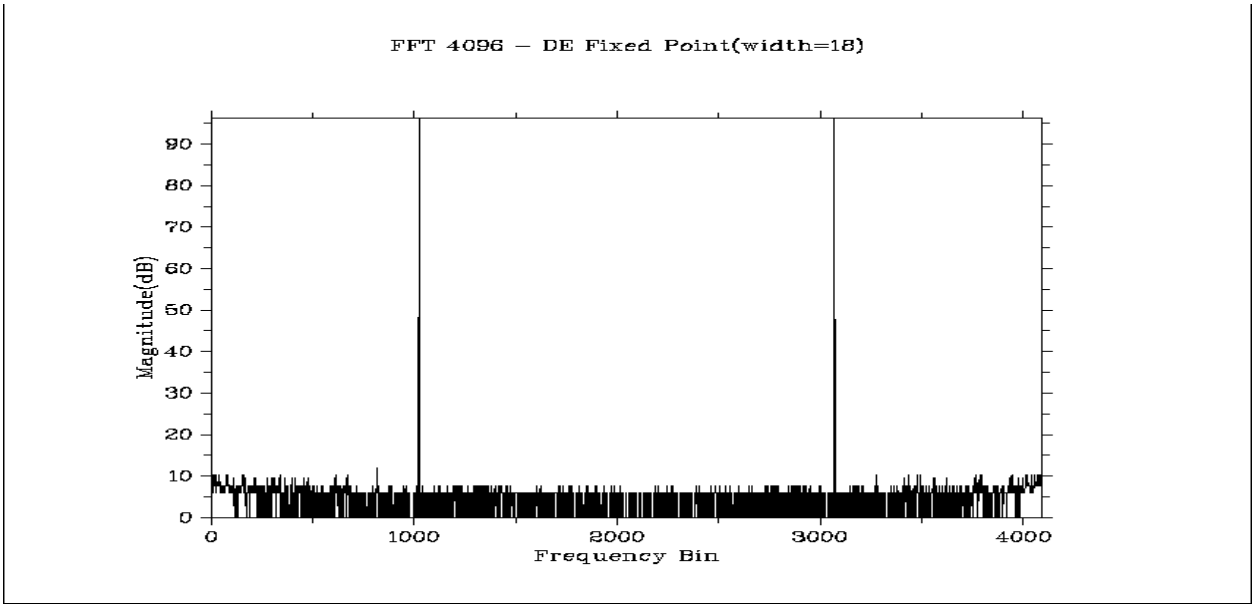
The FpFFT is also utilized in DE's ultra-long and 2D FFT engines, producing results far more accurate than fixed point solutions.

The FpFFT Core is a ParaCore Architect™ IP Core, making configuration option specification at compile time via parameters.

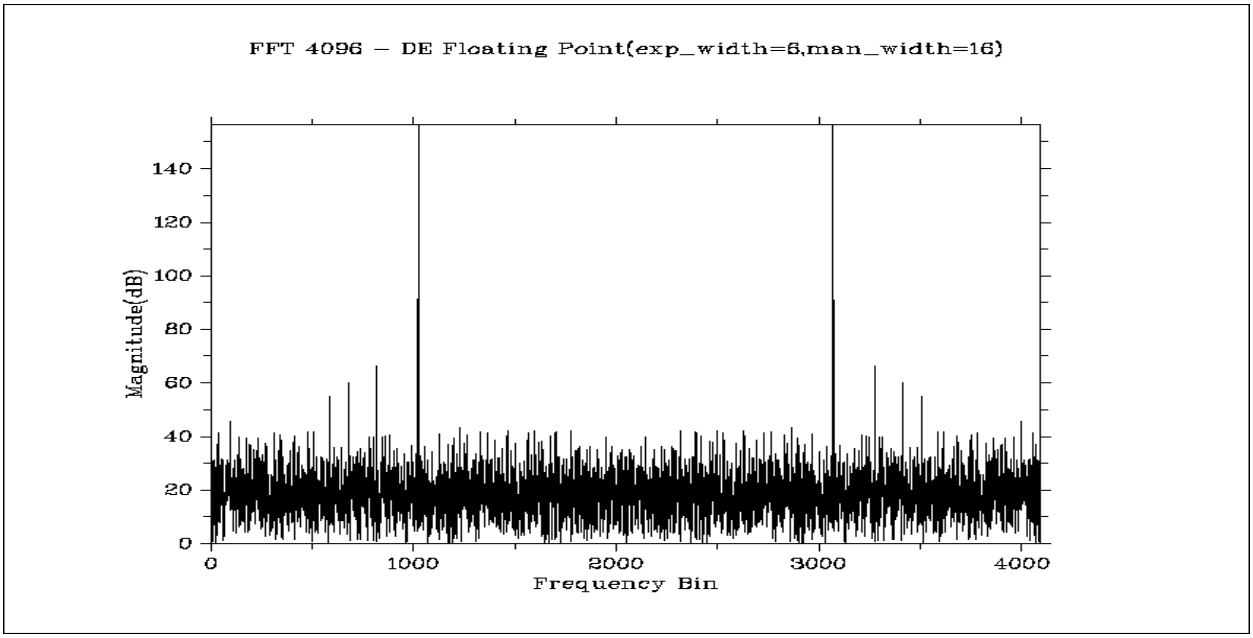
Sample Plots

The following are the results of 4096 point FFTs on the following input signal:

sig = 32,767 * sin(1.0/4 * 2 * pi * x) + 1.00 * sin(1.0/5 * 2 * pi * x) +
0.50 * sin(1.0/6 * 2 * pi * x) + 0.25 * sin(1.0/7 * 2 * pi * x)
x is a sequence from 0 to 4047. Note there are four signals present, a full scale (16 bit), a 2, 1 and 0.5 bit peak to peak signals.



Required scaling to capture full scale signal causes loss of small signals.



All signals well above noise in output with only 6 bit exponent and 16 bit mantissa.

Virtex II area Usage

The following table shows the device usage for several configurations of a 6 bit exponent and 16 bit mantissa FFT. This configuration gives a dynamic range of +/- 2**31 and 16 bits of precision.

Xilinx Virtex II 150 MHz – Complex Inputs – exponent == 6, mantissa == 16					
Length	***Butter-flies***	***Slices***	***Mult18x18***	***Block RAMs***	***Rate (uS)***
1024	1	3,982	4	10	34.13
1024	4	15,231	16	31	8.53
1024	8	30,183	32	62	4.27
2048	1	4,334	4	20	75.09
2048	4	16,903	16	31	18.77
2048	8	33,768	32	62	9.39
4096	1	5,117	4	36	163.84
4096	4	19,639	16	39	40.96
4096	8	38,934	32	62	20.48
Xilinx Virtex II 150 MHz – Complex Inputs – Single Precision					
1024	1	6,166	16	18	34.13
2048	4	26,295	64	39	18.77

FftEngine Performance

Any number of butterflies can be instantiated, all in parallel. Each butterfly increases the performance. The following formula can be used to determine how fast the DE FpFFT Core can process data.

$$Cycles = N * log2(N)/(bfs * 2)$$

Where Cycles are the number of clock cycles to complete the FFT, N is the length of the FFT and bfs is the number of butterflies instantiated. For example a 1024 point FFT with 8 butterflies would be completed in:

$$Cycles = N * log2(N)/(bfs * 2)$$
$$Cycles = 1024 * log2(1024)/(8 * 2)$$
$$Cycles = 640$$

With a 150 Mhz clock, the transform would be completed in 4.27uS. Another way to look at the speed of this FFT is 4.27 uS / 1024 is 4.17 nS per sample or 240 MSPS (mega samples per second).

Availability – Shipping

