Please stay tuned for today's webcast

"*FPGA Design For Complex Products*"

Microwaves&RF **Wireless Systems Design** **Mentor Graphics** **XILINX®**

The presentation will begin at 1:00 p.m. ET

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How this webcast will work

- **Questions**
  - Box in lower left corner
  - Ask them as they occur to you
- **Slides**
  - Enlarge
  - Download/print
- **Volume control**
  - Can be adjusted within Windows Media Player and RealPlayer; or
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FPGA Design For Complex Products

November 16, 2004

FPGA Design For Complex Products

HOST - **John Blyler**, Sr. Editor, *WSD magazine*

MODERATOR - **Clive "Max" Maxfield**

SPECIAL GUEST - **Tom Dillon**, *President, Dillon Engineering*

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➤**Juergen Jeager**, *Group Director, Channel Marketing*
➤**David Wiens**, *Director of Business Development*
➤**Shawn McCloud**, *Product Marketing Manager, Catapult C*

➤**Steve Lass**, *Director of Software Product Marketing*
➤**Andy DeBaets**, *Sr. Director Systems Application Engineering*

Question 1

**All FPGA vendors provide free design tools to their customers.
So why should I, as a designer, pay for FPGA design tools from EDA vendors?**
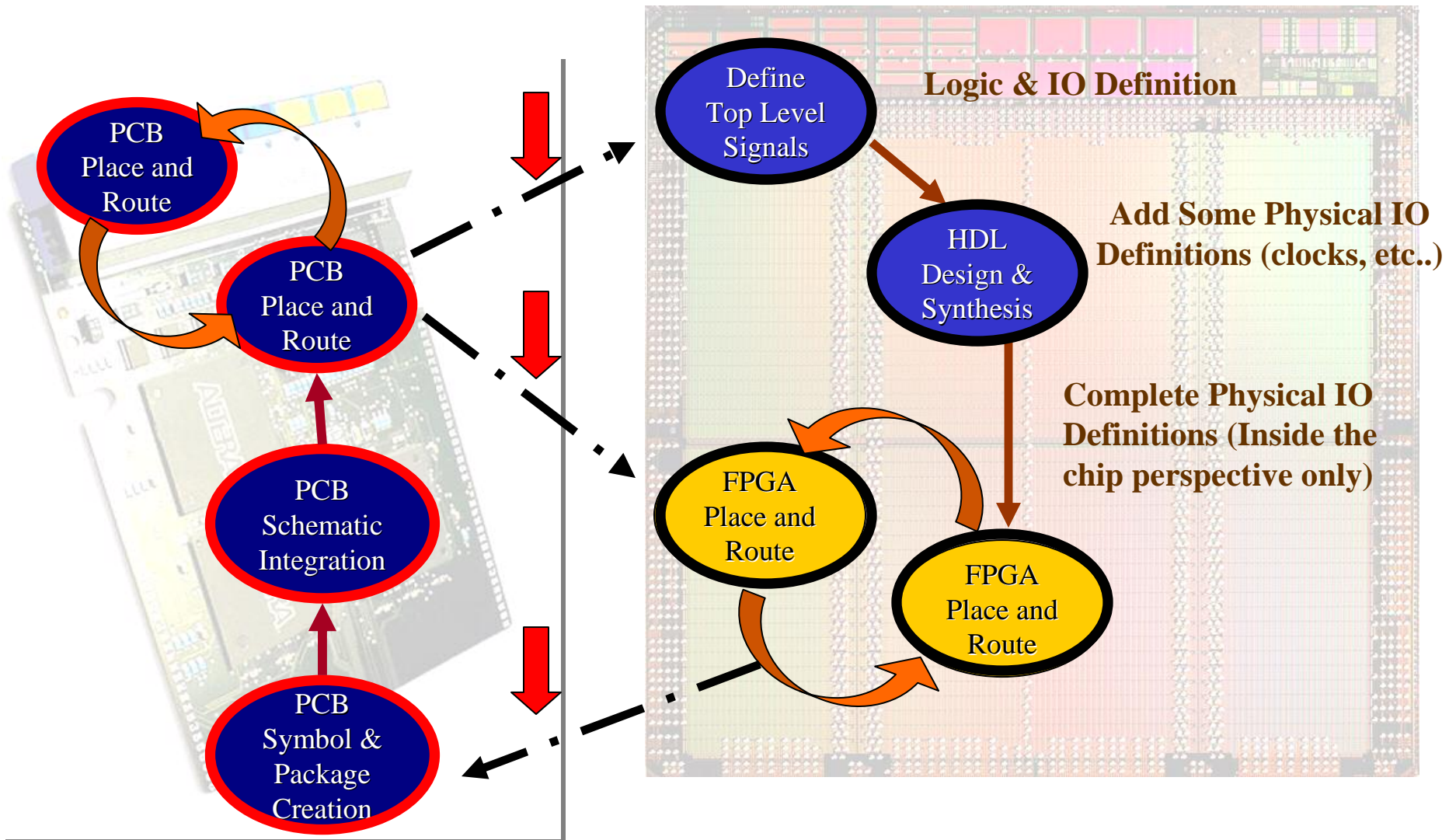
FPGA Vendor vs. EDA Tools

- **Most Xilinx SW engineers working on:**
  - device support, performance, runtime
- **Xilinx does not have all tools**
  - PCB, signal integrity, formal verification
- **Main overlap is in synthesis**
  - low-end synthesis is a commodity
  - EDA vendors must add value
    - flow, integration, analysis, performance

All FPGA vendors provide free design tools to their customers. So why should I, as a designer, pay for FPGA design tools from EDA vendors?

- Vendor-independent solutions provide highest ROI, most flexibility, highest quality of results
- FPGA vendors provide low-cost design sw to customers, but there's a catch – *Entrapment*
    - Learning new FPGA vendor tool flows
    - Very difficult to re-use flows with new FPGAs
- Mentor's solutions combine vendor-independent design creation, verification, synthesis, and board integration for the most comprehensive FPGA flow
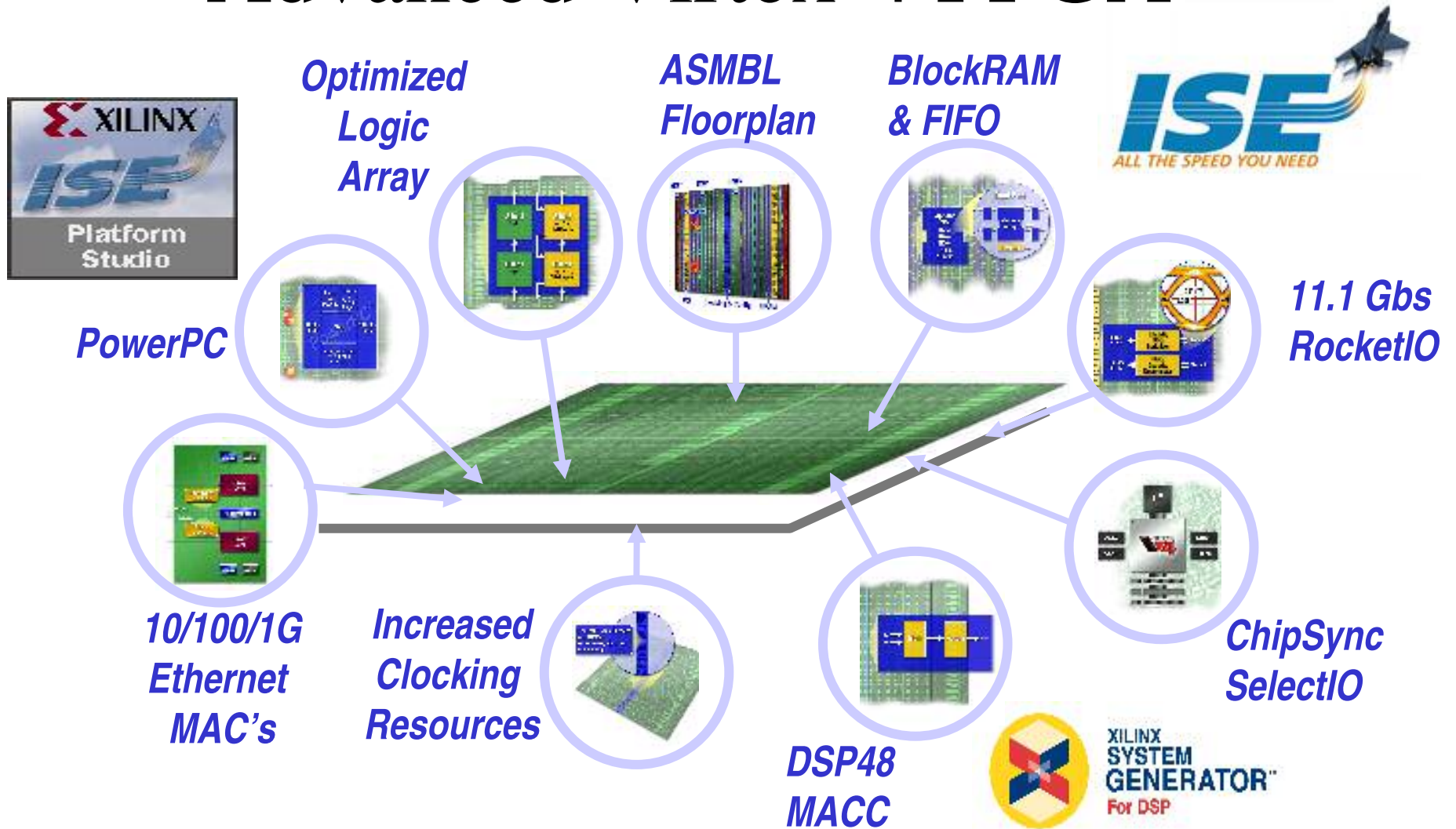
All FPGA vendors provide free design tools to their customers. So why should I, as a designer, pay for FPGA design tools from EDA vendors?

PCB Place and Route

PCB Place and Route

PCB Schematic Integration

PCB Symbol & Package Creation

Define Top Level Signals

Logic & IO Definition

HDL Design & Synthesis

Add Some Physical IO Definitions (clocks, etc..)

Complete Physical IO Definitions (Inside the chip perspective only)

FPGA Place and Route

FPGA Place and Route

Mentor Graphics®

Question 2

Is system level design a reality for FPGAs?

Advanced Virtex-4 FPGA

Optimized Logic Array

ASMBL Floorplan

BlockRAM & FIFO

PowerPC

11.1 Gbs RocketIO

10/100/1G Ethernet MAC's

Increased Clocking Resources

ChipSync SelectIO

DSP48 MACC

System Design Enabled with Advanced Features!

Is system-level design a reality for FPGAs?
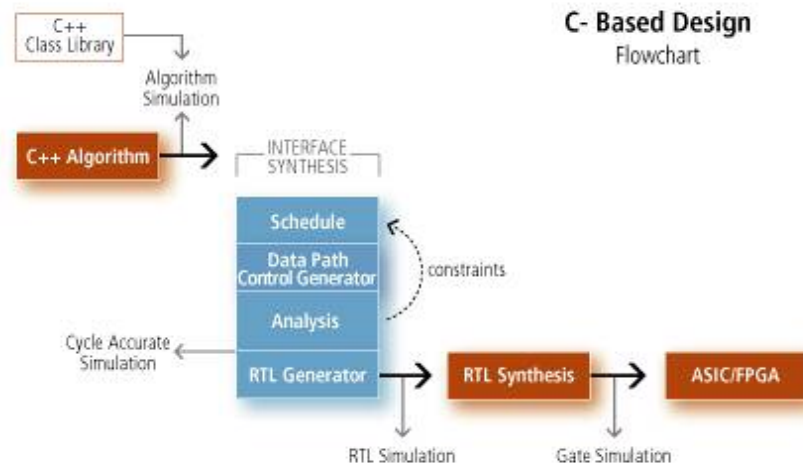
CPU Dominant
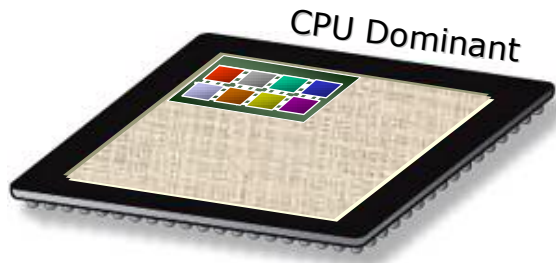
- •CPU based with little HW acceleration
- •Memory occupying majority of available space

IP Dominant

- •CPU based with HW accelerators
- •Combination of existing IP + new design intent

Dedicated Hardware

- •Highly application specific
- •Dense, optimized pipeline stages

Software ← - - - - - - - - - - - - - - - → **Hardware**

C-Based Design
Makes ESL Possible

C- Based Design
Flowchart

C++ Class Library

C++ Algorithm

Algorithm Simulation

INTERFACE SYNTHESIS

Schedule

Data Path Control Generator

Analysis

RTL Generator

constraints

Cycle Accurate Simulation

RTL Synthesis

ASIC/FPGA

RTL Simulation

Gate Simulation

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Question 3

What are some of the challenges posed by these new high-end FPGAs when you put them on the printed circuit board.

What are some of the challenges posed by these new high-end FPGAs when you put them on the printed circuit board?

System performance

- Multi-gigabit transceiver signals
  - 3-11 Gbps asynchronous (serial)
- Timing-sensitive synchronous (parallel) signals
- More system design constraints
- New simulation requirements
- Advanced PCB fabrication

Designer productivity

- Multiple FPGAs per board
- Multiple design iterations
- Manual process integration
- Disconnected design teams
- High-density / pin-count FPGAs
  - Interdependency between FPGA pin-outs and PCB interconnect
  - PCB routability
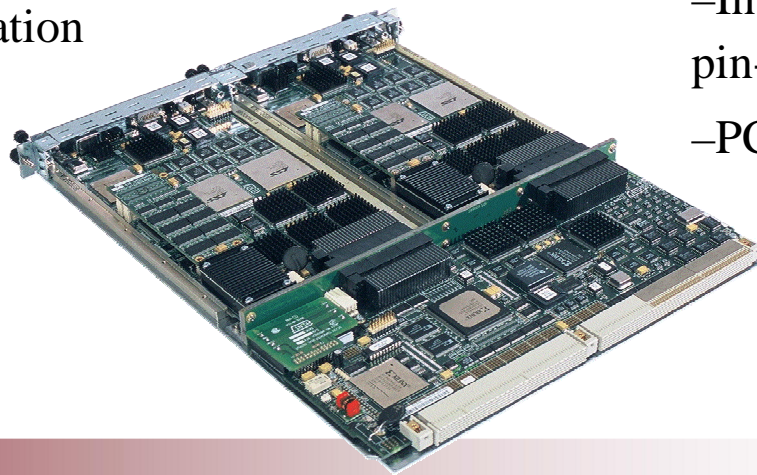
Question 4

What to do when the design for a complex product doesn't work in the FPGA?

- **RTL Simulation, should be done already, make sure it still works.**
- **Gatesim (post P&R), run full simulation with RTL simulation testbench.**
- **Analyze timing, make sure all paths are covered and meet timing.**
- **Clock strategy, all clocks global and domain crossing bullet proof.**
- **Test I/O without logic, verify data integrity on/off FPGA.**
- **On chip testing, either route out signals to logic analyzer or use something like ChipScope.**
- **Must have means to apply test data to design and capture results, preferably sampling the data at many points within the flow.**
- **Start with simple cases to isolate and fix errors.**

What to do when the design for a complex product doesn't work in the FPGA?

- Fairly broad question, could have several meanings…
- Doesn't work at all: Use design tools
  - Check your simulations, simulate with back annotated timing delays (ModelSim)
  - Make sure all signals have timing constraints
  - Did "Done" go high? (did the part configure?)
  - Do you have power? What do your clocks look like? (Hyperlynx)
- Mostly works: Use debug tools
  - Logic analyzer: Chipscope Pro, or Agilent FPGA Dynamic Probe are powerful tools
  - Chipscope Pro VIO (Virtual IO core) allows real-time interaction
- Works except when you build 100 and put them in the oven…
  - Frequently signal integrity issues
  - Example: with latest FPGA technology, edge rates are such that all loads are transmission lines. So for LVCMOS, LVTTL use 8 ma or 12 ma drivers. Don't use 16 ma or 24 ma drivers. Use controlled impedance versions of these drivers (DCI). Higher current drivers are not giving you faster signals but are giving you more signal integrity issues
  - Example: pay extra attention to your ground vias and your pcb layer stack-ups. The ground layer should be as close to the FPGA as possible to minimize the ground via inductance

What to do when the design for a complex product doesn't work in the FPGA?

- Functionality issues
  - Take advantage of design analysis capabilities built into today's FPGA design tools (e.g. static timing analysis, clock-tree analysis, etc.)
- Performance/timing issues
  - Apply physical synthesis and analysis techniques to achieve faster, more predictable timing closure
- Timing closure Issues introduced by the PCB
  - Interconnect
    - Reduced signal integrity due to impedance discontinuities, attenuation, crosstalk
    - Timing skew due to line delays
  - Devices
    - Poor decoupling
    - Resistor terminations too far away

Question and Answer Session

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