fft_64k

Overlapped Parallel-Butterfly FFT / IFFT Core, 64 to 65,536 Points

Product Datasheet · AMD UltraScale+ FPGAs

Features

- Transform length 64 to 65,536 points (2^6 to 2^{16}), selected **per frame** at run time
- FFT or IFFT selected per frame
- Built-in input overlap: 0, 1/8, 1/4, 3/8, 1/2, 5/8 or 3/4. Only new samples are supplied; overlapped samples are reused internally
- Per-rank divide-by-2 scaling, selected per frame
- Continuous streaming: one complex sample per clock in, four per clock out, natural order
- 32 parallel radix-2 butterflies
- Data width 12 to 32 bits per component (24 by default); twiddle width 16 to 24 bits
- 275 MHz on Kintex UltraScale+, slowest (-1) speed grade
- No processor bus or registers: all settings travel with the frame
- Sticky overflow and error status
- Delivered with a bit-accurate fixed-point model and a self-checking testbench; RTL verified bit-exact against the model

Key specifications

Transform length	64 – 65,536 points, per frame
Algorithm	Radix-2 decimation in time, 32 butterflies
Direction	FFT / IFFT, per frame
Overlap	0 to 3/4 in eighths, per frame
Input rate	1 sample/clock, continuous (275 MSPS)
Output rate	4 samples/clock, natural order (up to 1.1 GSPS)
Arithmetic	Fixed point, two's complement, rounding at each rank
Data width	12 – 32 bits/component, build time
Twiddle width	16 – 24 bits/component, build time
Clock	Single clock, 275 MHz
Reference device	Kintex UltraScale+ KU5P, -1
Language	SystemVerilog / Verilog
Tools	AMD Vivado 2025.2

Block Diagram

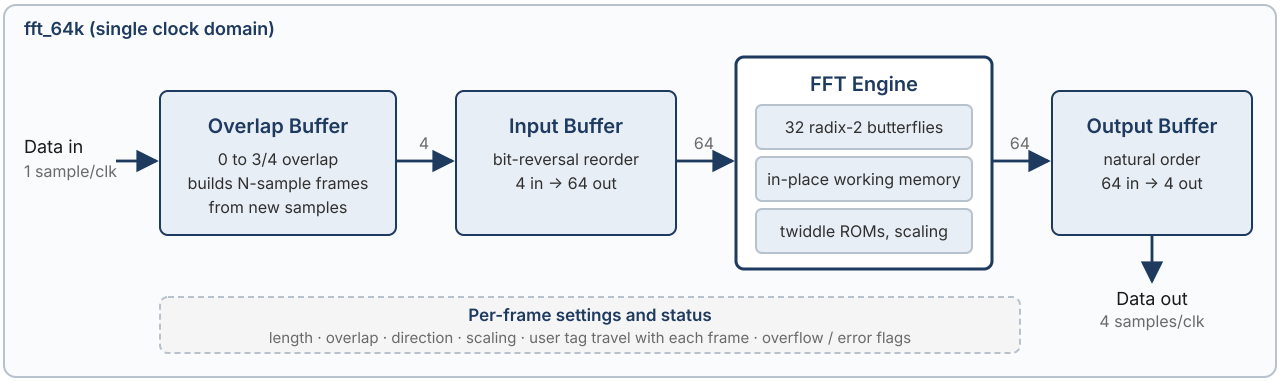

Figure 1. fft_64k block diagram. Bus widths are in complex samples.

Description

fft_64k is a run-time configurable, fixed-point FFT/IFFT core for AMD UltraScale+ FPGAs. Every frame can use a different transform length, direction, overlap and scaling, with no software in the loop and no reconfiguration time between frames.

The core takes a continuous stream of one complex sample per clock. Overlapped transforms are handled inside the core: the user supplies only the new samples for each frame, and the core reuses the overlapped samples from the previous frame. Results leave the core in natural order, four samples per clock, so at 3/4 overlap the output runs at full duty.

Interface

All ports are registered at the core boundary. Widths shown are for the default configuration (24-bit data, 64K maximum length).

Port	Dir	Width	Description
`clk`	in	1	Core clock, rising edge
`rst_n`	in	1	Active-low reset; asynchronous assert, synchronous release
`syncIn`	in	1	Frame start, one cycle before the frame's first new sample
`lenSelIn`	in	5	$\log_2(N)$, 6 to 16
`ovlpIn`	in	3	Overlap in eighths, 0 to 6 (0 to 3/4)
`dirIn`	in	1	1 = FFT, 0 = IFFT
`scaleIn`	in	16	Bit r = 1 divides the output of rank r by 2
`miscIn`	in	1+	User tag, returned with the frame on `miscOut`
`dataIn`	in	48	Complex sample: real in upper half, imaginary in lower half
`dataValidIn`	in	1	`dataIn` holds a valid sample
`syncOut`	out	1	Output frame start, one cycle before the first output word
`lenSelOut, ovlpOut, dirOut, miscOut`	out	as inputs	The output frame's settings, valid on the `syncOut` cycle
`dataOut`	out	192	Four complex samples per clock, natural order; lane j holds sample 4c + j
`dataValidOut`	out	1	High for the N/4 cycles following `syncOut`
`arithOverflowOut`	out	1	Sticky: a butterfly result overflowed
`errorOut`	out	5	Sticky error flags (buffer overflow, missed frame, etc.)

Streaming protocol

- Assert `syncIn` for one cycle with the frame settings, then supply the frame's M = N·(1 − overlap) new samples on consecutive cycles.
- Frames may be back-to-back: the next `syncIn` may share the cycle of the current frame's last sample. Idle cycles between frames are allowed.
- Frames leave the core one-to-one and in order. `miscIn` is a convenient place for a frame counter.
- There is no back-pressure. Downstream logic accepts four samples per clock while `dataValidOut` is high.
- After reset, and after a change of transform length, the first frame uses overlap 0.

Performance

Throughput

The core accepts one sample per clock continuously at every supported length and overlap, and produces one frame every $M = N \cdot (1 - \text{overlap})$ clocks.

N	Frames/s, overlap 0	Frames/s, overlap 1/2	Frames/s, overlap 3/4
1,024	268,555	537,109	1,074,219
4,096	67,139	134,277	268,555
16,384	16,785	33,569	67,139
65,536	4,196	8,392	16,785

Table 1. Frame rate at 275 MHz, continuous input.

Supported overlap

N	64	128	256	512 – 65,536
Maximum overlap	1/4	1/2	5/8	3/4

Latency

Latency from a frame's `syncIn` to its `syncOut` is approximately $M + N/4 + (N/64) \cdot (\log_2 N - 1)$ clocks, plus a fixed overhead of a few tens of clocks. It does not depend on the frame rate.

N	Overlap	syncIn → syncOut	syncIn → last output
1,024	0	5.2 µs	6.1 µs
1,024	3/4	2.4 µs	3.3 µs
4,096	0	21.2 µs	24.9 µs
4,096	3/4	10.0 µs	13.7 µs
16,384	0	86.6 µs	101.5 µs
16,384	3/4	41.9 µs	56.8 µs
65,536	0	354 µs	413 µs
65,536	3/4	175 µs	235 µs

Table 2. Approximate frame latency at 275 MHz, excluding the fixed overhead.

Numerical Performance

Data is stored at the same width at every rank, with no word growth in memory. Each butterfly forms its complex product at full precision, applies the rank's optional divide-by-2, rounds to the data width and detects overflow. Scaling is chosen per rank and per frame: full scaling (every rank) cannot overflow and gives FFT/N; partial scaling (for example every second rank) keeps more precision for wideband signals.

N	Tone, −0.4 dBFS, full scaling	Noise, −12 dBFS, full scaling	Noise, −12 dBFS, every 2nd rank
1,024	104 dB	96 dB	106 dB
4,096	100 dB	90 dB	105 dB
16,384	95 dB	84 dB	104 dB
65,536	89 dB	78 dB	103 dB

Table 3. Estimated signal-to-quantization-noise ratio at the default widths (24-bit data, 18-bit twiddles). Each bit of data width changes these figures by about 6 dB until the twiddle width becomes the limit.

Resource Utilization

Resource	Used	Available	Utilization
CLB LUTs	96,263	216,960	44.4%
CLB registers	61,697	433,920	14.2%
Block RAM tiles (36 Kb)	363	480	75.6%
UltraRAM	16	64	25.0%
DSP48E2	96	1,824	5.3%

Table 4. Post-route, out-of-context, default configuration (24-bit data, 18-bit twiddles, 64K maximum length) on xcku5p-ffva676-1-e, Vivado 2025.2. Timing met at 277.8 MHz. A smaller maximum length or narrower data reduces memory use.

Deliverables

- Synthesizable RTL source and implementation constraints
- Bit-accurate fixed-point model (Octave/MATLAB, and C with an Octave/MATLAB interface)
- Self-checking SystemVerilog testbench, test-vector generator and complete test vectors
- Simulation and synthesis scripts for Vivado, with reference build reports
- User guide and full design document

> **Evaluation and licensing.** The full design document, covering detailed timing, configuration options and integration guidance, is available on request. Contact **info@dilloneng.com**.

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